REMARKS

Applicant thanks the Examiner for the careful review of this application. Claims 6, 13 and 22 were cancelled without prejudice. Claims 1, 8, 10, 18, 21 and 23 were amended to further clarify aspects of the invention. No new matter has been added. Therefore, claims 1, 3-5, 7-8, 10-12, 14-21 and 23 remain pending in this application.

REJECTIONS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claim 22 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, the phrase "the polysilicon layer thickness" lacked antecedent basis.

Claim 22 was incorporated into independent claim 21 and "the polysilicon layer thickness" was amended to recite --a thickness of the polysilicon layer--. Applicant respectfully requests that the Examiner withdraw the rejection of cancelled claim 22, now incorporated into independent claim 21.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1, 3, 4, 6, 8, 10, 13 and 15-20 were rejected under 35 U.S.C § 103(a) as being unpatentable over Ryum (U.S. Patent No. 6,337,494) in view of Kubota (U.S. Patent No. 6,323,530).

Claims 5, 7, 12 and 14 were rejected under 35 U.S.C § 103(a) as being unpatentable over Ryum (U.S. Patent No. 6,337,494) in view of Kubota (U.S. Patent No. 6,323,530) and further in view of Streetman (Solid State Electronic Devices).

Applicant respectfully traverses these rejections.

Ryum apparently discloses a super self-aligned heterojunction bipolar transistor that possibly is capable of miniaturizing an element, possibly simplifying the process step thereof

without using a trench isolation process and a possibly sophisticated selective epitaxial growth (SEG) processes. According to this invention, the sophisticated isolation and the SEG techniques are derived by using apparently simple and popular processes. The base layer has multi-layer structure being made of a Si, an undoped SiGe, a SiGe doped a p-type impurity in-situ and Si. Also, the selective epitaxial growth is not required. Thus, it possibly can be less prone to a flow of leakage current or an emitter-base-collector short effect.

Kubota apparently discloses an optical semiconductor device that includes a semiconductor substrate having an active layer, a semiconductor mesa stripe formed on the semiconductor substrate, a dummy mesa stripe formed on the semiconductor substrate, an insulating layer formed to fill up a gap between the semiconductor mesa stripe and the dummy mesa stripe, a main electrode formed on the semiconductor mesa stripe, and an extension electrode formed on top surfaces of the insulating layer and the dummy mesa stripe. The extension electrode is connected to the main electrode.

Streetman apparently discloses various techniques and materials useful for fabricating semiconductor integrated circuits.

Ryum, Kabota and Streetman do not teach the elements of the invention as defined in independent claims 1, 8, 18 and 20, alone or in combination. The invention as recited in independent claims 1, 8, 18 and 20 is directed to an apparatus and method for forming a super self-aligned bipolar transistor wherein the horizontal etching is executed to a distance greater than a distance of the polysilicon thickness. Advantageously, this allows for precise control of the transistor gain and frequency response – a characteristic that is lacking in the cited art. The horizontal etch distance claim elements, of dependent claims 6, 13 and 21, were incorporated into independent claims 1, 8 and 20, respectively.

The Examiner cites Ryum's disclosure, that the conducting layer of the base electrode is formed such that its height is equal to that of the collector (column 4, lines 9-12 and 43-49; and figure 3, where layers 12 and 12-1 are base layers and 14 and 2 are emitter and collector layers,

respectively), as being equivalent to etching the polysilicon layer a horizontal distance greater than the thickness of the polysilicon layer. Applicant respectfully points out that Ryum is referring to forming the base electrode to a thickness equal to that of the collector thickness. Further support can be found in Ryum column 8, lines 63-67 ("Thereafter, the conducting film 11 is further etched using the first masking layer 6 as an etching stopper, wherein the conducting film 11 and the polysilicon masking layer 7 are also etched as the etched thickness of the conducting film 11, as shown in FIG. 4(H).").

Claims 3-5, 7, 10-12, 14-17, 21 and 23 depend directly or indirectly from independent claims 1, 8, 18 and 20 and are therefore allowable for at least the same reasons as set forth for independent claims 1, 8, 18 and 20. Claims 6, 13 and 22 were previously cancelled without prejudice. Withdrawal of the rejections of claims 1, 3-5, 7-8, 10-12, 14-21 and 23 are respectfully requested.

Applicant respectfully traverses the rejections of the originally submitted claims and reserves the right to re-introduce them and claims of an equivalent scope in a continuation application. If the undersigned agent has overlooked a relevant teaching in any of the references, the Examiner is requested to point out specifically where such teaching may be found.

CONCLUSION

Applicant believes that all pending claims are allowable and a Notice of Allowance is respectfully requested.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,
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APPENDIX A – VERSION WITH MARKINGS TO SHOW CHANGES MADE – CLAIMS

1. (Twice amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein [the step of providing a horizontal etching determines that the dimensions of the base region are wider then the doped collector region and the emitter region;]said horizontally etched layer is a polysilicon layer and is etched a distance greater than a thickness of said polysilicon layer;

providing a wet etching to remove a final one of said multiple layers; [and]

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

8. (Twice amended) A super self-aligned bipolar transistor, comprising:

a semiconductor substrate having a buried collector region;

multiple layers above said collector region;

an emitter window mask above said multiple layers;

a doped collector region wherein the width of the doped collector region are equal to the emitter window mask width;

a horizontal etched region of one of said multiple layers, wherein [the dimensions of the horizontally etched region determine that the dimensions of the base region are wider than the doped collector region and the emitter region;] said horizontally etched region is a polysilicon region and extends a distance greater than a thickness of said polysilicon region;

a base region above said collector region in the horizontally etched area; and

an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontally etched region determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

11. (Once amended) The apparatus as described in claim [9]10 further comprising an oxide surface and a Nitride layer above said layers of surface oxide and polysilicon.

18. (Twice amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing a first oxide layer, a polysilicon layer and a second oxide layer above said collector region;

providing a Nitride emitter window mask above said oxide and polysilicon layers;

providing a wet etching with hydrofluoric acid solutions to etch first and second oxide layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of said polysilicon layer, wherein [the dimensions of the horizontally etched region determine that the dimensions of the base region are wider than the doped collector region and the emitter region of the transistor;]said horizontal etching is etched a distance greater than a thickness of said polysilicon layer;

[providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;]

providing a base region above said collector region in the horizontally etched area[;] wherein the base region extends horizontally beyond the doped collector region; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

21. (Once amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein [the step of providing a horizontal etching determines that the dimensions of the base region are wider than the dimensions of the doped collector region and the emitter region;]said horizontal etching is performed to a distance greater than a thickness of said polysilicon and whereby said distance may be conformed to provide desired electrical characteristics;

providing a wet etching to remove a final one of said multiple layers; [and]

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

23. (Once amended) The method of claim [22]21 wherein the desired electrical characteristics are transistor gain and frequency response.